0127570.020601

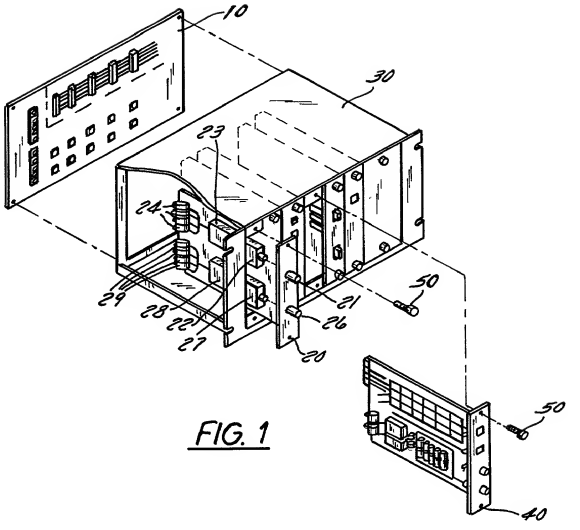


FIG. 1

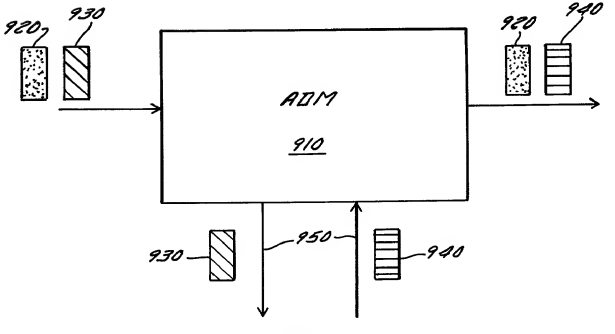


FIG. 9

211
212
213
214
215
216
210
DATA SOURCE
AUDIO
VIDEO
RS232
E-NET
T1
INTERFACE
SIGNAL
DIGITIZER
SYNCHRONIZER
SUBMUX
TDM
MULTIPLEXER
217
OPTICAL TX
ELECTRIAL TO OPTICAL CONVERTOR
ANALOG
CONDITIONED ANALOG
A/D
PARALLEL TO SERIAL CONVERSION WITH 10B/12B ENCODER
230
221
222
223
224
225
226
227
OPTICAL RX
TDM
DEMULTIPLEXER
CLK
RECOVER
SUBMUX
DESYNCHRONIZER + TIMER
D/A
INTERFACE
FILTER
AUDIO
VIDEO
RS232
E-NET
T1
DATA SINK
220
OPTICAL TO ELECTRICAL CONVERTOR
SERIAL TO PARALLEL CONVERSION WITH 12B/10B DECODING & CLOCK RECOVERY
DIGITAL TO ANALOG

FIG. 2

T0980 30* 02677760

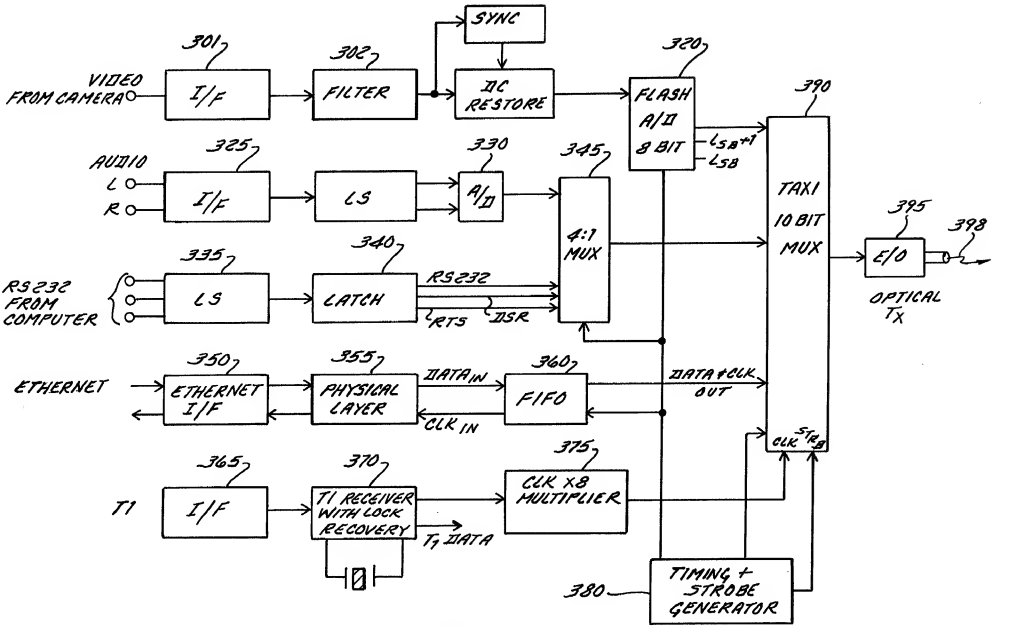


FIG. 3

Translation of PCT/US97/07760

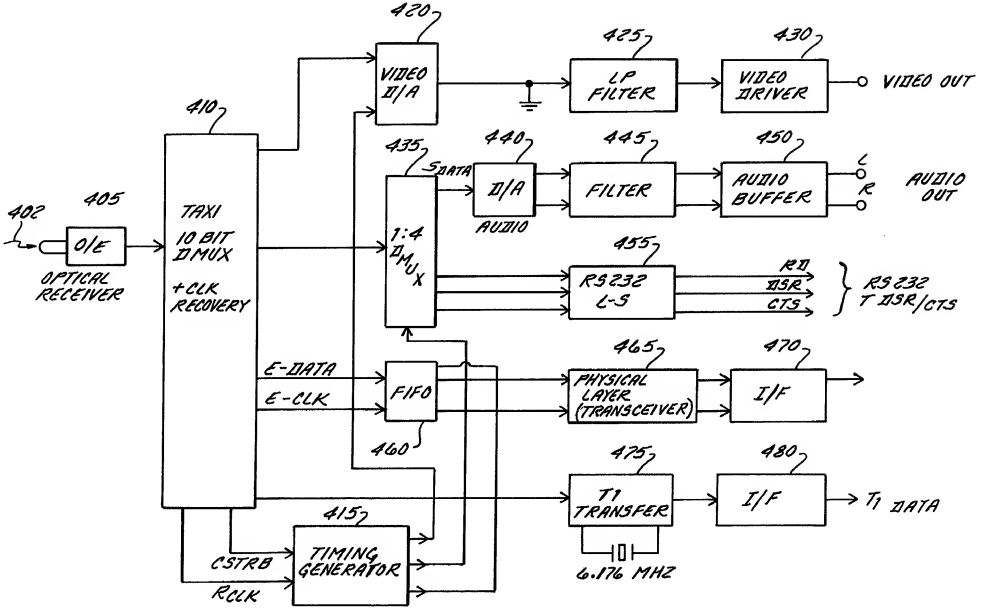


FIG. 4

TD9020 "0767770"

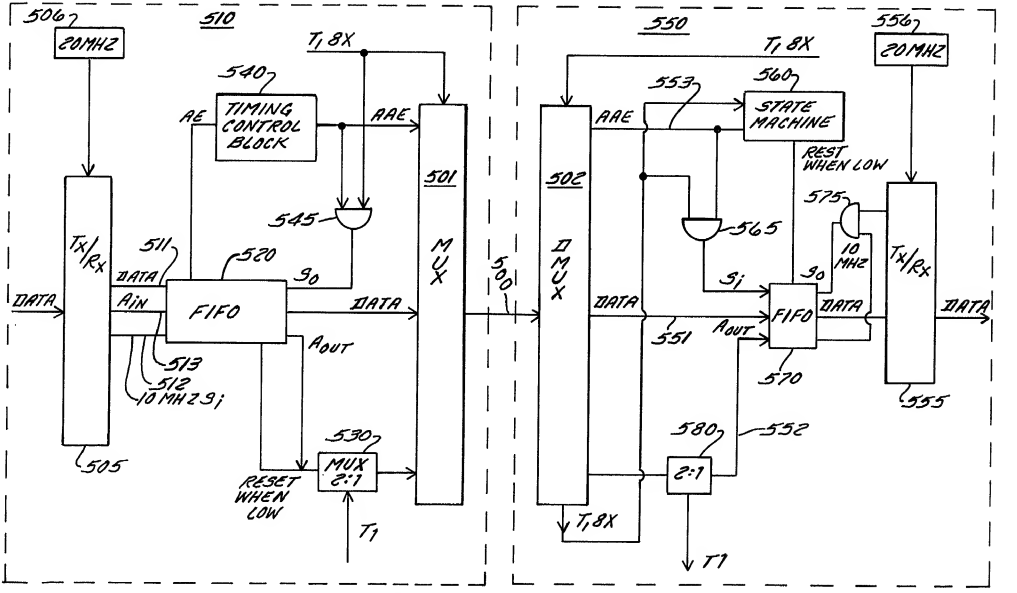
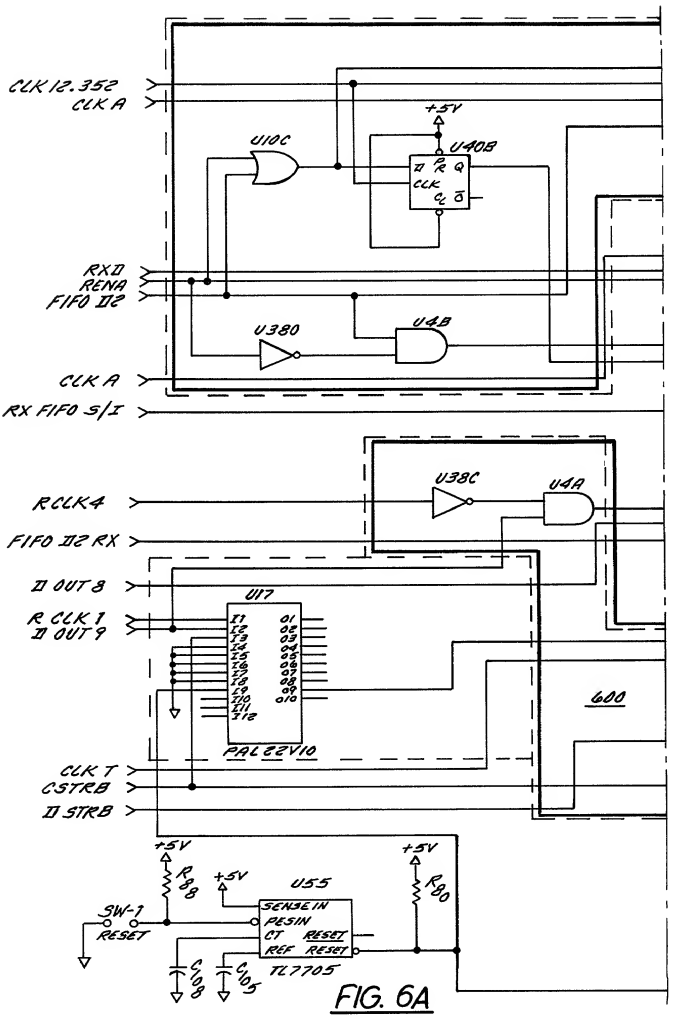
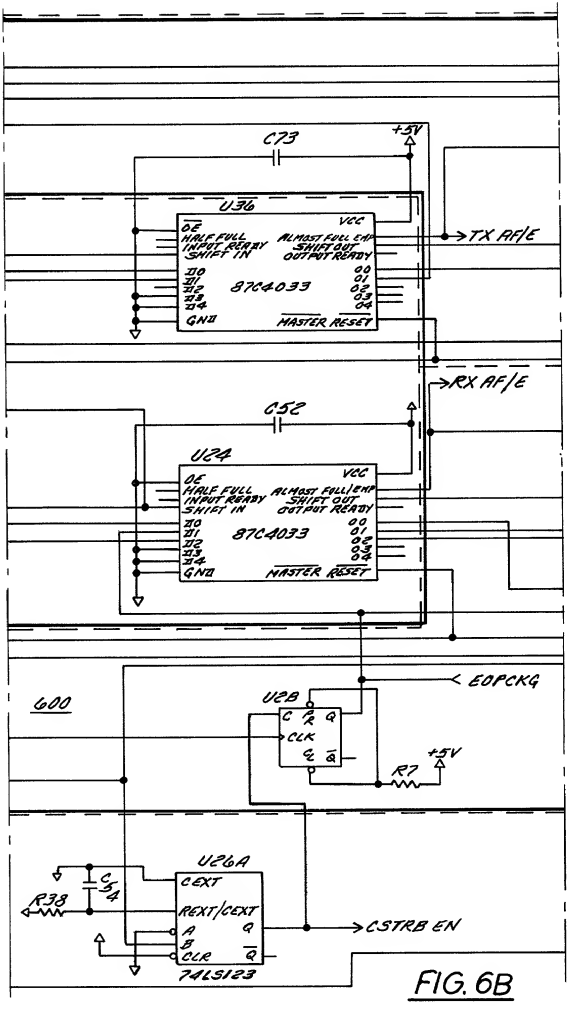


FIG. 5


CLK 12.352
CLK A
+5V
U10C
U40B
D
CLR
Q
CLK
PRE
Q
RXD
RENA
FIFO D2
U38D
U4B
CLK A
RX FIFO S/I
U38C
U4A
RCLK4
FIFO D2 RX
D OUT 8
U17
R CLK 1
D OUT 9
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
I12
O1
O2
O3
O4
O5
O6
O7
O8
O9
O10
600
PAL22V10
CLK T
CSTRB
D STRB
+5V
+5V
+5V
SW-1
RESET
U55
SENSE IN
RESIN
CT RESET
REF RESET
TL7705
FIG. 6A


C73
+5V
U36
OE
HALF FULL
INPUT READY
SHIFT IN
VCC
ALMOST FULL/EMP
SHIFT OUT
OUTPUT READY
I10
I11
I12
I13
I14
GND
87C4033
O0
O1
O2
O3
O4
MASTER RESET
TX AF/E
RX AF/E
C52
U24
600
U28
C
R
Q
CLK
S
Q
EOPCKG
R7
+5V
U26A
CEXT
REXT/CEXT
A
B
CLR
C34
R38
CSTRB EN
74LS123
FIG. 6B

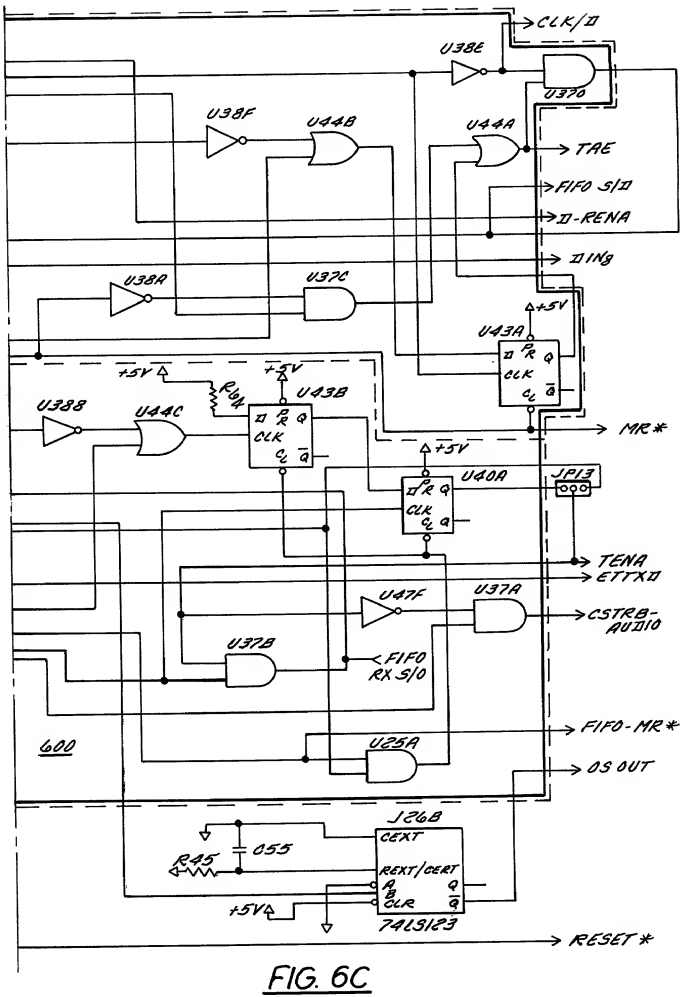

CLK/D
U38E
U37D
U38F
U44B
U44A
TAE
FIFO S/D
D-RENA
D ING
U38A
U37C
+5V
U43A
D PR Q
CLK
CL Q
+5V
+5V
R164
U43B
U38B
U44C
MR*
+5V
U40A
JP13
TENA
ETTXD
U47F
U37A
CSTRB-AUDIO
U37B
FIFO RX S/O
FIFO-MR*
600
U25A
OS OUT
J26B
CEXT
C55
R45
REXT/CEXT
A
B
CLR
Q
Q
+5V
74LS123
RESET*

FIG. 6C

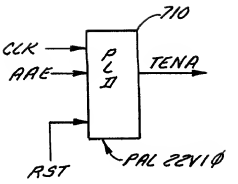


FIG. 7A

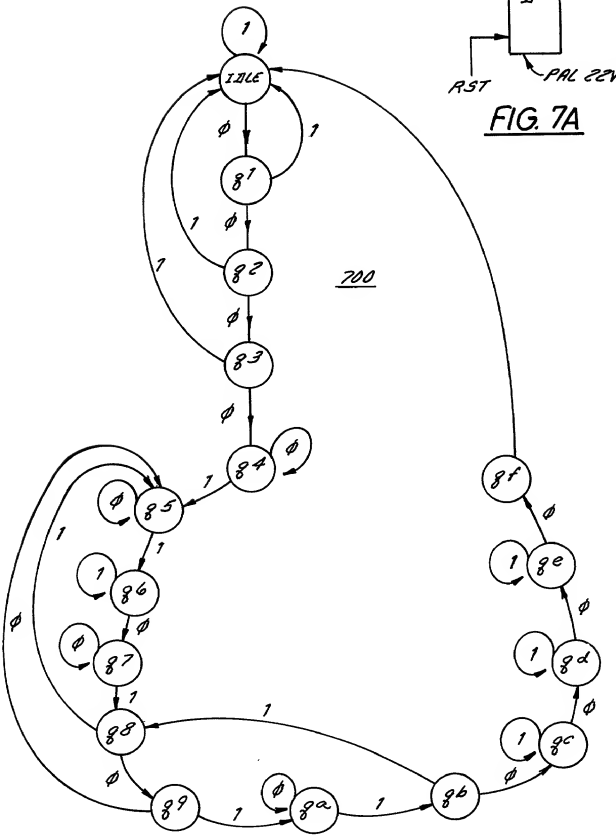


FIG. 7B

09777208.002601

09777970.020603

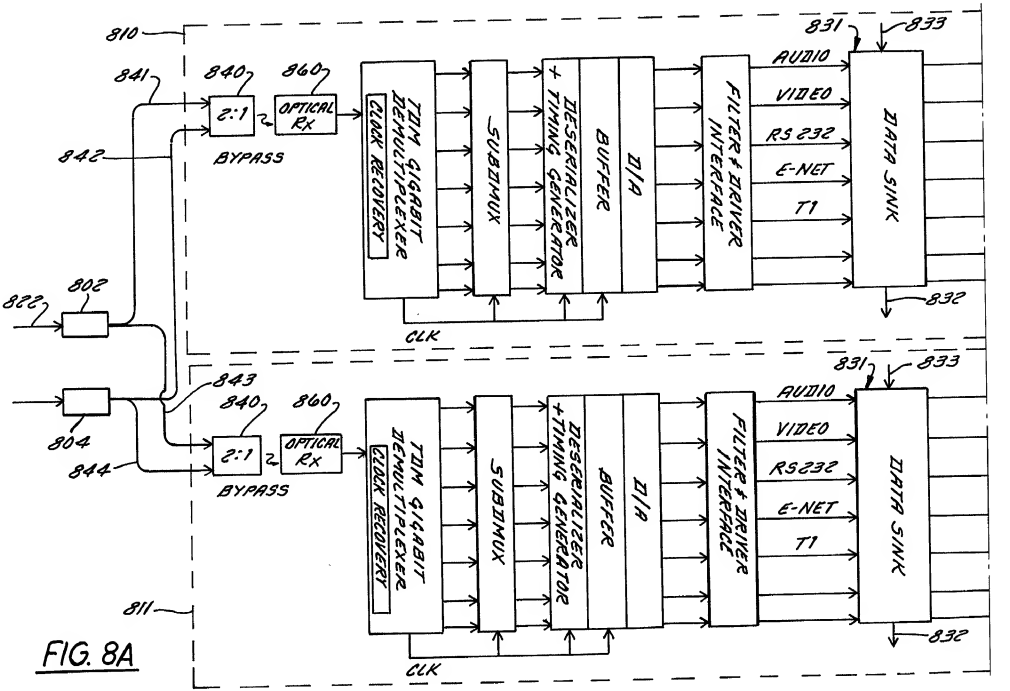


FIG. 8A

09779780.060801

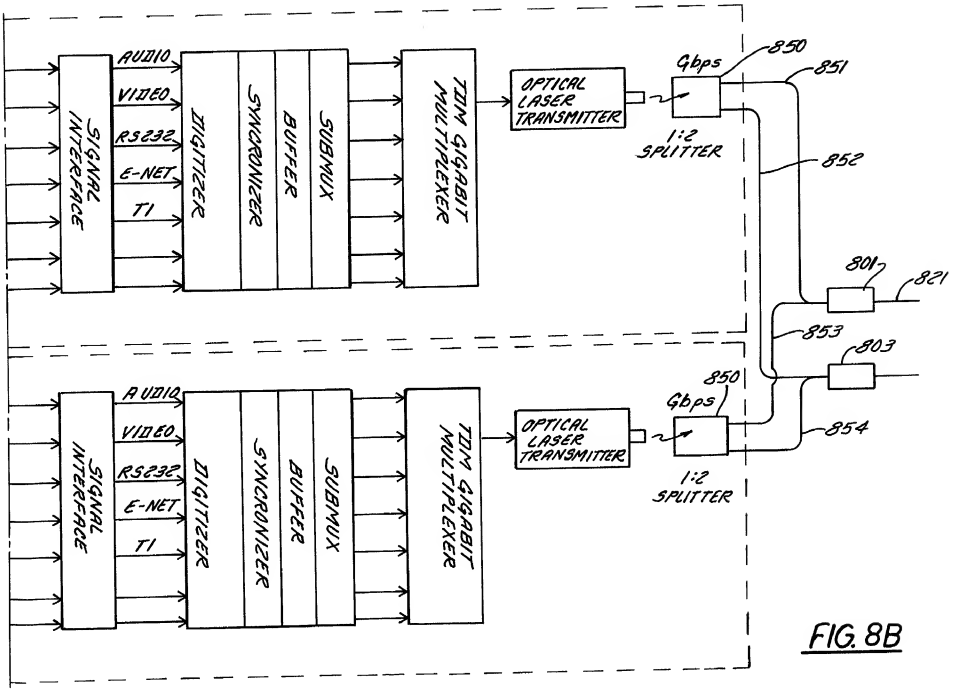


FIG. 8B

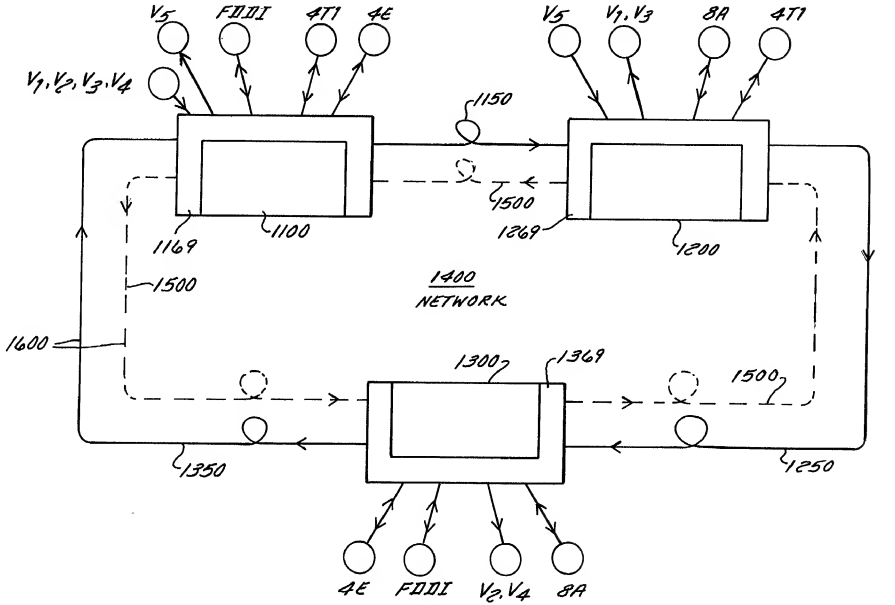

V5
FDDI
4T1
4E
V1, V2, V3, V4
1150
V5
V1, V3
8A
4T1
1500
1169
1100
1369
1200
1400
NETWORK
1500
1600
1300
1369
1500
1350
1250
4E
FDDI
V2, V4
8A

FIG. 10

US 6,977,970 B2

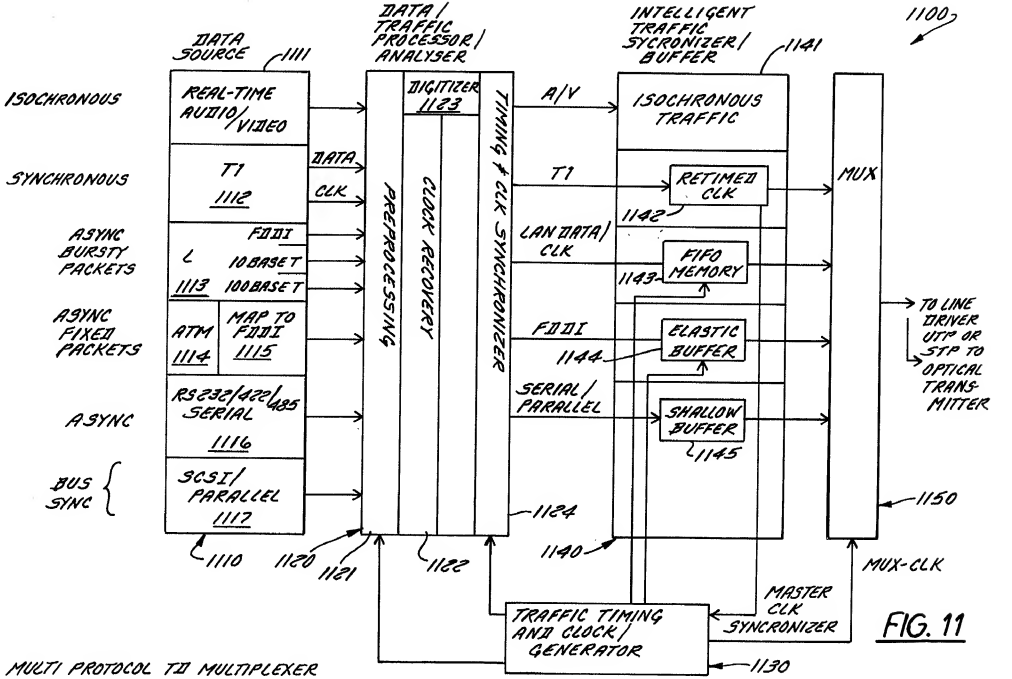


FIG. 11

097779?0 .020801

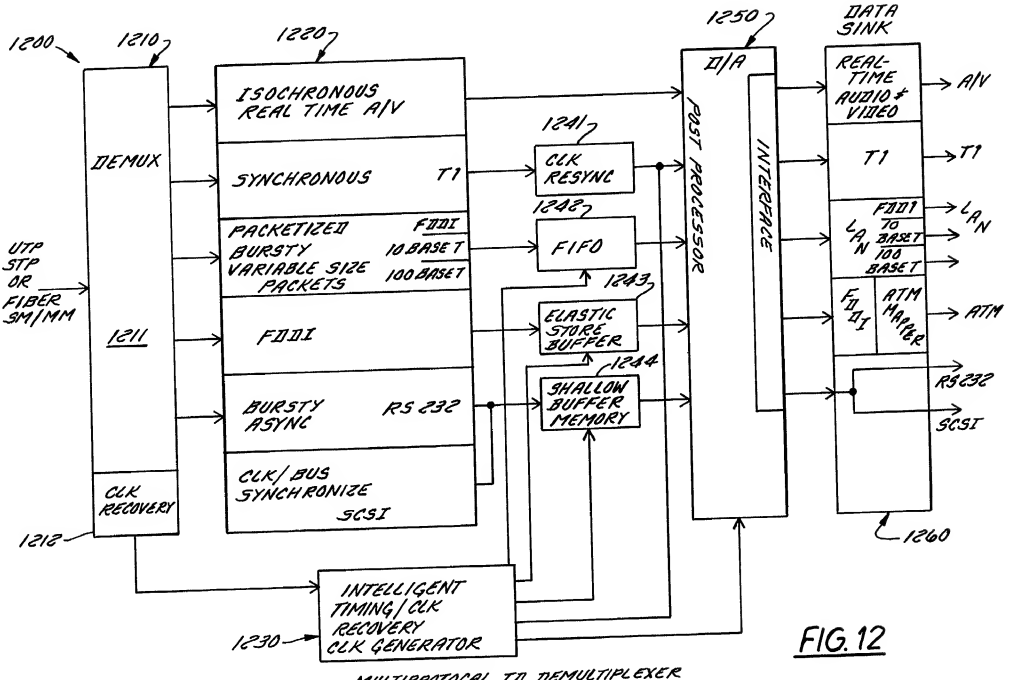


FIG. 12

MULTIPROTOCAL TI DEMULTIPLEXER

DATA TYPE	MULTIPLEXER/ DEMULTIPLEXER INTERFACE REQUIREMENT	DATA RATE	TIMING SENSITIVITY
AUDIO/ VIDEO MULTIMEDIA	• CONTINUOUS SAMPLING • LOCK MATCHING • MINIMUM BUFFERING	VARIABLE BIT RATE IN COMPRESSED MODE UNCOMPRESSED DEPENDS ON RESOLUTION & SAMPLING RATE	AUDIO/ VIDEO SYNCHRONIZATION
RS232/422/485 SERIAL ASYNCHRONOUS SCSI PARALLEL BUS SYNCHRONIZED	CAN USE BUFFER OR LOW SPEEDS USE OVERSAMPLING REQUIRE FIFO MEMORY	VARIBLE 10Kb/s → 10Mb/s VARIABLE → 40 MBYTE/s	BAUD RATES NEED MATCHING INTERLOCKED HANDSHAKE BUS TIMING SYNCHRONIZATION
T1	NEED DIRECT MATCHING OF T1 CLK WITH MUX SYNCHRONIZATION OF MASTER CLOCK	1.544 Mb/s	CLOCK/RECOVERY VERY STRICT TIMING REQUIRE CLK 1.544± 32 PPM
LAN NETWORK — FDDI	NEED CLOCK RECOVERY MINIMUM BUFFER AND STRICT DATA RATE MATCHING USING SHALLOW FIFO	100 Mb/s	CLOCK RECOVERY REQUIRED ELASTIC BUFFER
LAN NETWORK — 10 BASE T		10 Mb/s	CLOCK RECOVERY NEEDED
LAN NETWORK — 100 BASE T		100 Mb/s	CLOCK RECOVERY NEEDED
WIDE AREA STI/STS ATM	PRECISE NEED CLOCK RECOVERY AND DEFRAMING WITH TRANSFER TO PACKET	51.84/155.5 OC1/OC3 Mb/s	TIME/STAMP REQUIREMENT CLOCK CORRECTION

FIG. 13A

DELAY/LATENCY SENSITIVITY	TRAFFIC TYPE / DATA STREAM	APPLICATIONS	REMARKS TYPE OF CHANNEL
CONSTANT FOR MINIMUM JITTER	CONSTANT BIT RATE LAMINAR BIT STREAM	MULTIMEDIA TELECONFERENCING VIDEO CONFERENCING SECURITY	ISOCHRONOUS
JITTER REQUIREMENT (NOT VERY TIGHT)	VARIABLE BIT RATE	COMPUTER TO COMPUTER / PERIPHERAL COMPUTER TO MEMORY	ASYNCHRONOUS BUS SYNCHRONOUS
MINIMUM JITTER REQUIREMENT FOR VOICE MIN. ACCEPTABLE LATENCY ~ 150 ms	CONSTANT BIT RATE	TELEPHONY WIDE AREA	SYNCHRONOUS
MAX. ELASTICITY FUNCTION OF NETWORK / TOKEN ROTATING TIMES	BURSTY ASYNCHRONOUS PACKETIZED	OPTICAL NETWORK IN BACKBONES	BURSTY PACKETIZED
COLLISSION DOMAIN LIMITED	ASYNCHRONOUS	LAN	ASYCHRONOUS
COLLISSION DOMAIN LIMITED	ASYNCHRONOUS	LAN	ASYCHRONOUS
VARIABLE LATENCY DEPENDING ON TRAFFIC MIN. LATENCY AND JITTER REQUIREMENT FOR VOICE/TELEPHONE AND MULTIMEDIA TRAFFIC	VBR: VARIABLE BIT RATE CBR: CONSTANT BIT RATE ABR: AVAILABLE BIT RATE ASYNCRONOUS TRANSFER MODE ASYNCHRONOUS	WIDE AREA NETWORK	CAN MAP ATM CELLS TO FIXI PACKETS AND THE TRANSFER SYNCHRONOUSLY

FIG. 13B

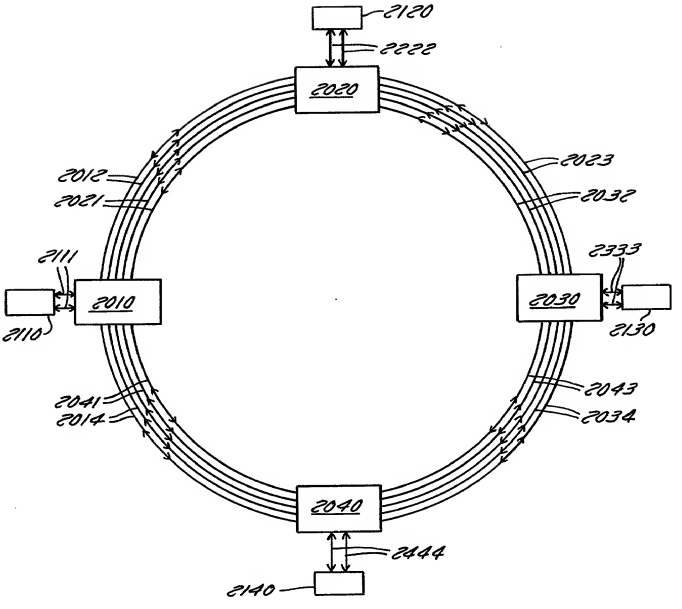

2120
2222
2020
2012
2021
2023
2032
2111
2333
2010
2030
2110
2130
2041
2014
2043
2034
2040
2444
2140

FIG. 14

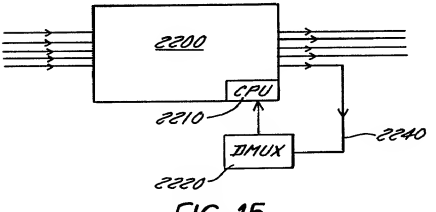

2200
CPU
2210
2240
IMUX
2220

FIG. 15

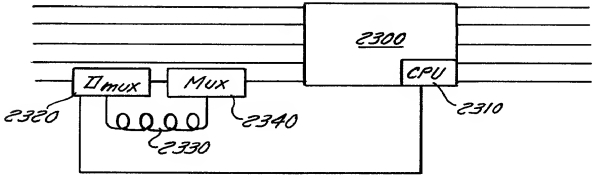

2300
CPU
Demux
Mux
2320
2340
2330
2310

FIG. 16

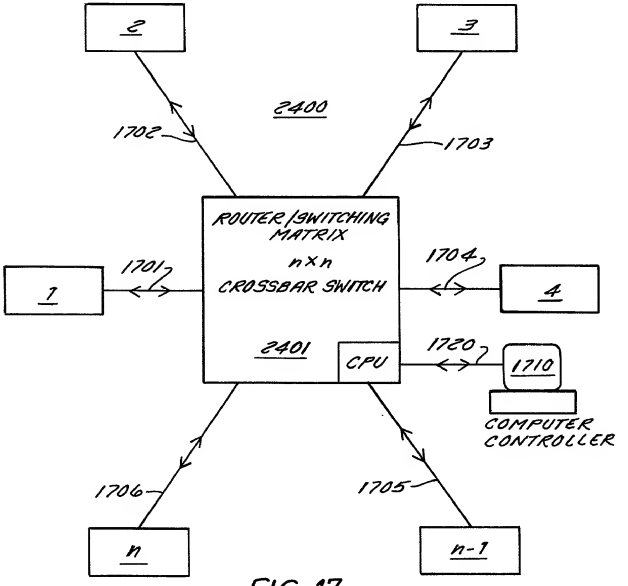

2
3
2400
1702
1703
ROUTER/SWITCHING MATRIX
nXn
CROSSBAR SWITCH
1701
1704
1
4
2401
CPU
1720
1710
COMPUTER CONTROLLER
1706
1705
n
n-1

FIG. 17

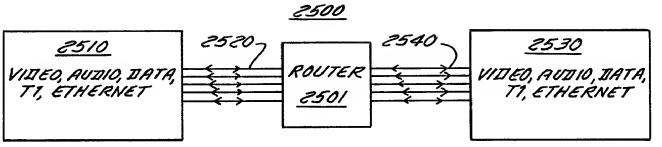

2500
2510
VIDEO, AUDIO, DATA, T1, ETHERNET
2520
ROUTER
2501
2540
2530
VIDEO, AUDIO, DATA, T1, ETHERNET

FIG. 18

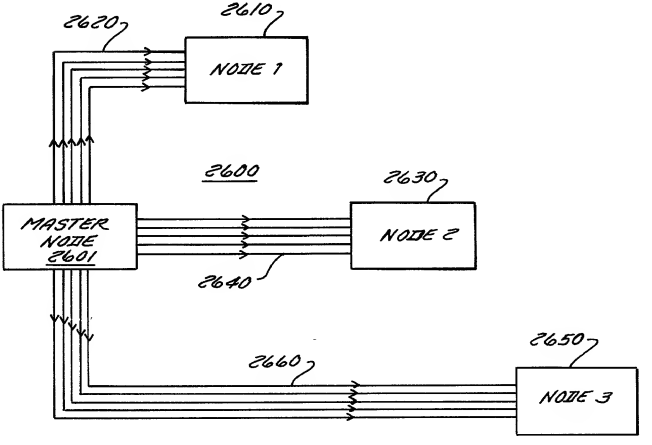

2620
2610
NODE 1
2600
2630
MASTER NODE 2601
NODE 2
2640
2650
2660
NODE 3

FIG. 19

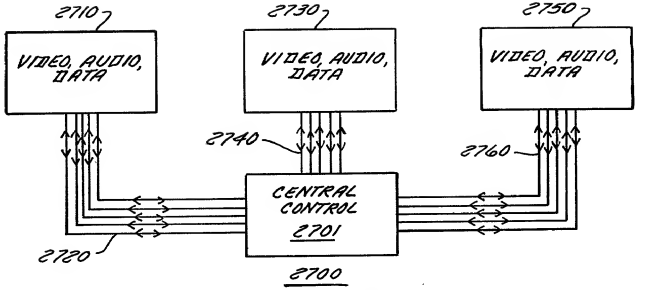

2710
VIDEO, AUDIO, DATA
2730
VIDEO, AUDIO, DATA
2750
VIDEO, AUDIO, DATA
2740
2760
CENTRAL CONTROL
2701
2720
2700

FIG. 20

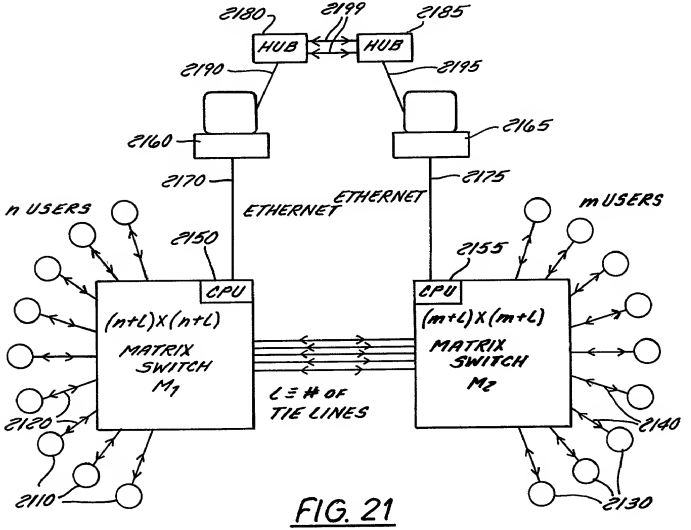

2180
2199
2185
HUB
HUB
2190
2195
2160
2165
2170
2175
ETHERNET
ETHERNET
n USERS
m USERS
2150
2155
CPU
CPU
(n+L)X(n+L)
MATRIX SWITCH M1
(m+L)X(m+L)
MATRIX SWITCH M2
L = # OF TIE LINES
2120
2140
2110
2130

FIG. 21

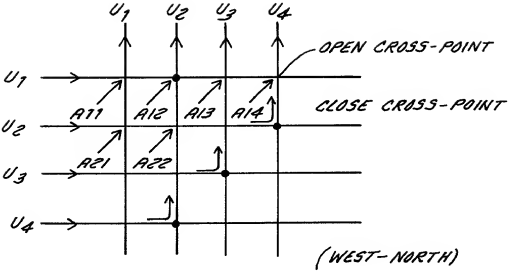

U1
U2
U3
U4
OPEN CROSS-POINT
CLOSE CROSS-POINT
A11
A12
A13
A14
A21
A22
(WEST-NORTH)

FIG. 22

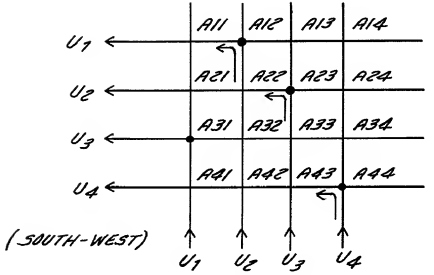

A11
A12
A13
A14
A21
A22
A23
A24
A31
A32
A33
A34
A41
A42
A43
A44
U1
U2
U3
U4
(SOUTH-WEST)

FIG. 23

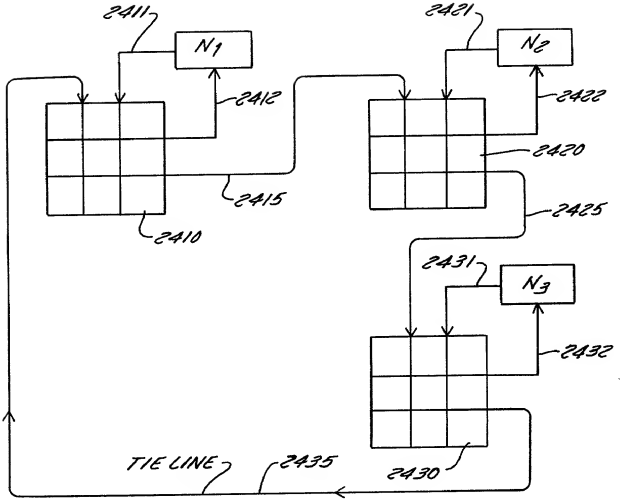

2411
N1
2412
2415
2410
2421
N2
2422
2420
2425
2431
N3
2432
2430
TIE LINE
2435

FIG. 24

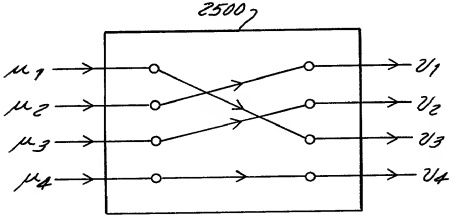

2500
μ1
μ2
μ3
μ4
v1
v2
v3
v4

FIG. 25

DRAFT 20020801

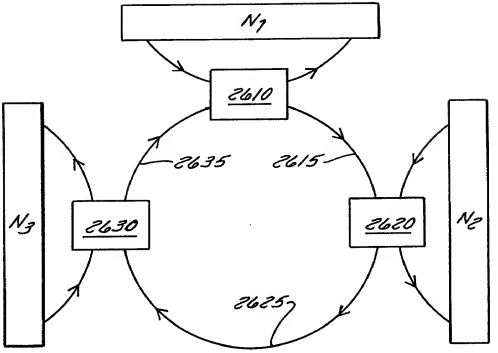


FIG. 26

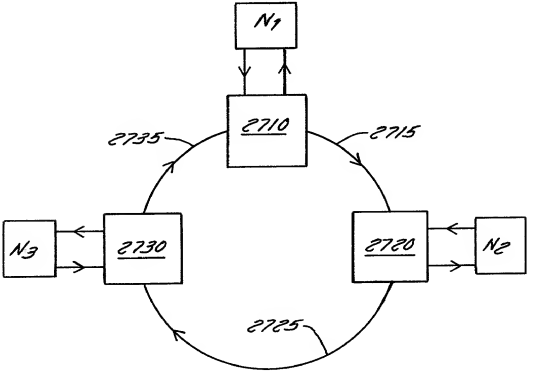


FIG. 27

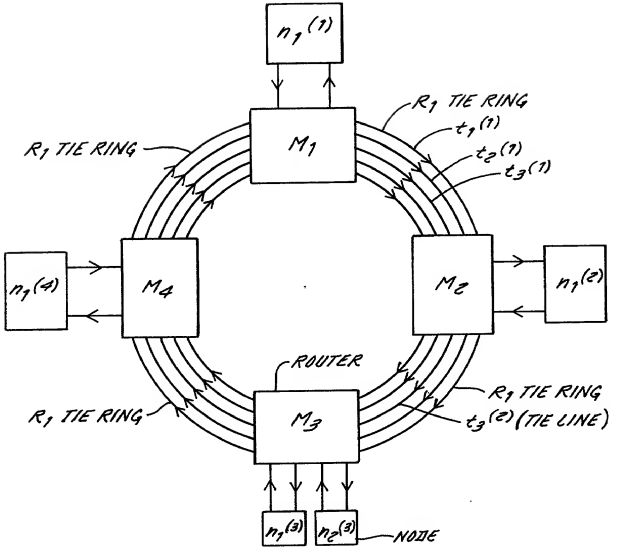

$n_1(1)$
R_1 TIE RING
$t_1(1)$
$t_2(1)$
$t_3(1)$
R_1 TIE RING
M_1
$n_1(4)$
M_4
M_2
$n_1(2)$
ROUTER
R_1 TIE RING
R_1 TIE RING
$t_3(2)$ (TIE LINE)
M_3
$n_1(3)$
$n_2(3)$
NODE

FIG. 28

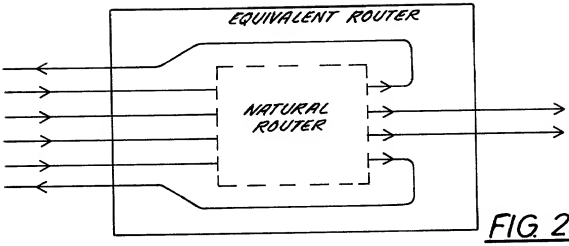


FIG. 29A

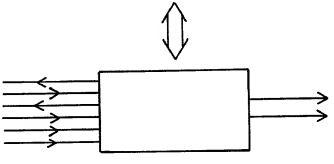


FIG. 29B

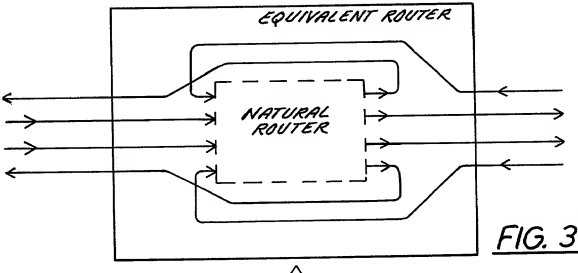


FIG. 30A

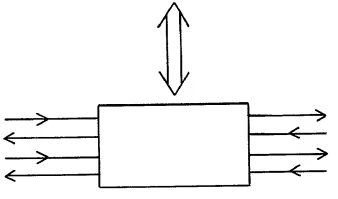


FIG. 30B

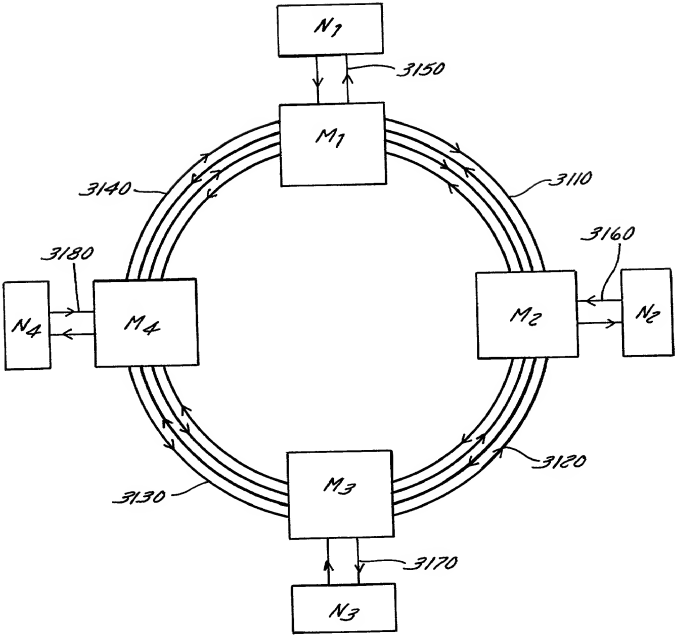


FIG. 31

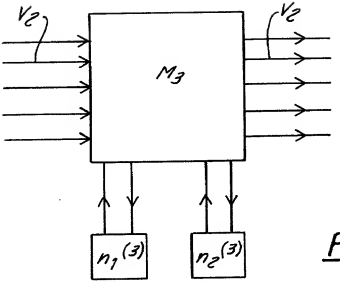


FIG. 32A

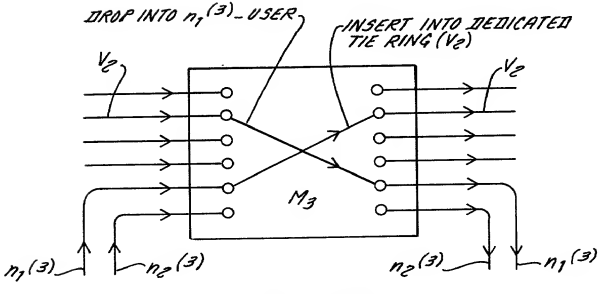


FIG. 32B

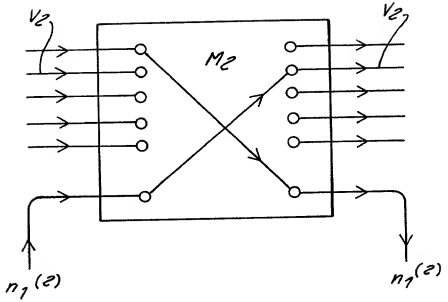


FIG. 32C

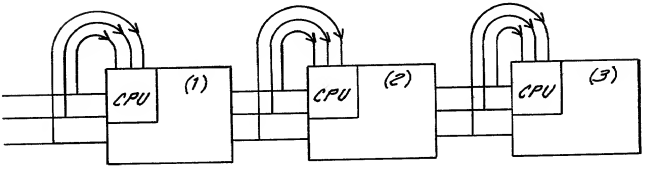


FIG. 32D

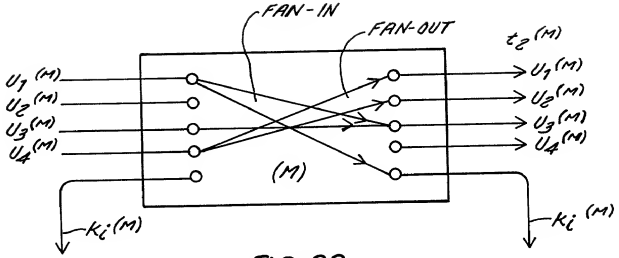

FAN-IN
FAN-OUT
$t_2^{(M)}$
$U_1^{(M)}$
$U_2^{(M)}$
$U_3^{(M)}$
$U_4^{(M)}$
(M)
$K_i^{(M)}$
$K_i^{(M)}$

FIG. 33

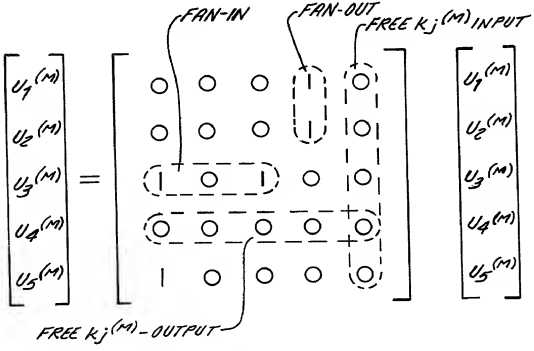

FAN-IN
FAN-OUT
FREE $K_j^{(M)}$ INPUT
$U_1^{(M)}$
$U_2^{(M)}$
$U_3^{(M)}$
$U_4^{(M)}$
$U_5^{(M)}$
=
FREE $K_j^{(M)}$ - OUTPUT

FIG. 34

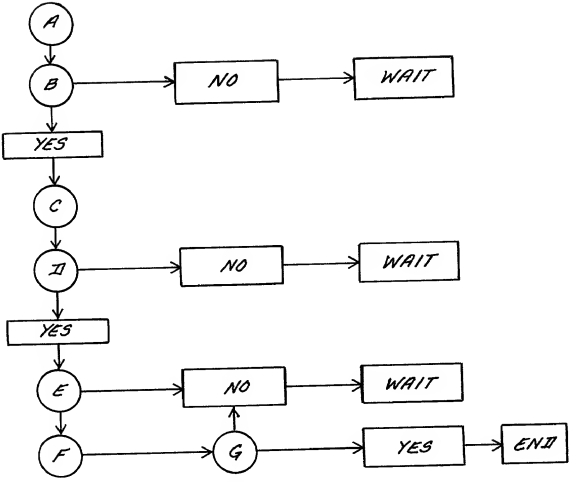

A
B
NO
WAIT
YES
C
D
NO
WAIT
YES
E
NO
WAIT
F
G
YES
END

FIG. 35

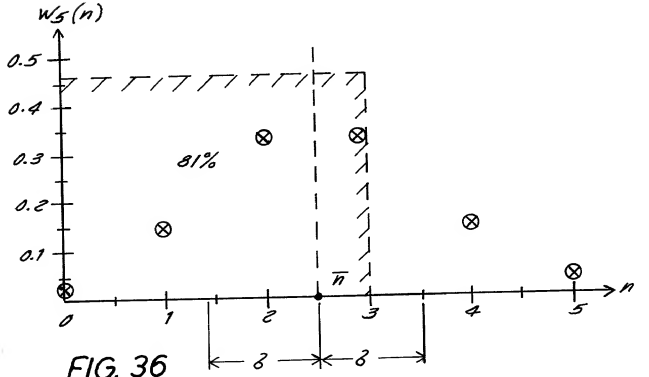

$W_S(n)$
0.5
0.4
0.3
0.2
0.1
81%
$\overline{n}$
n
0
1
2
3
4
5
δ
δ

FIG. 36

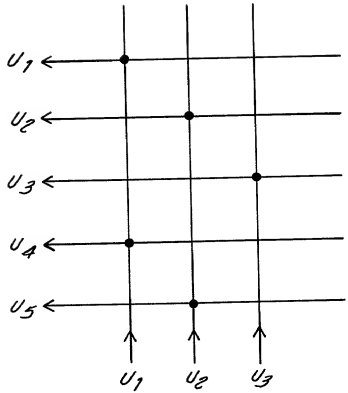


FIG. 37

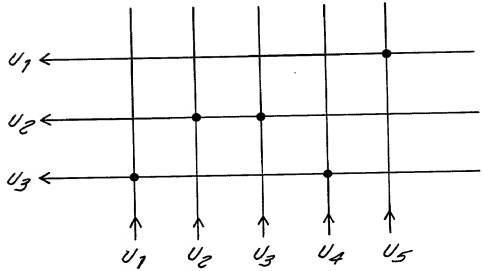


FIG. 38

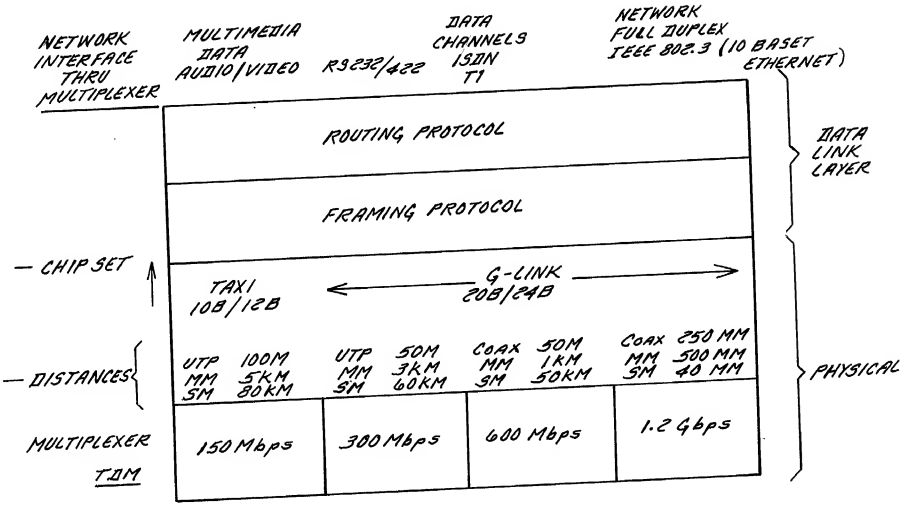

NETWORK INTERFACE THRU MULTIPLEXER
MULTIMEDIA DATA AUDIO/VIDEO
R3232/422
DATA CHANNELS ISDN T1
NETWORK FULL DUPLEX IEEE 802.3 (10 BASET ETHERNET)
ROUTING PROTOCOL
FRAMING PROTOCOL
DATA LINK LAYER
CHIP SET
TAXI 10B/12B
G-LINK 20B/24B
DISTANCES
UTP 100M MM 5KM SM 80KM
UTP 50M MM 3KM SM 60KM
COAX 50M MM 1KM SM 50KM
COAX 250 MM MM 500 MM SM 40 MM
PHYSICAL
MULTIPLEXER TDM
150 Mbps
300 Mbps
600 Mbps
1.2 Gbps

FIG. 39

09772970.020604

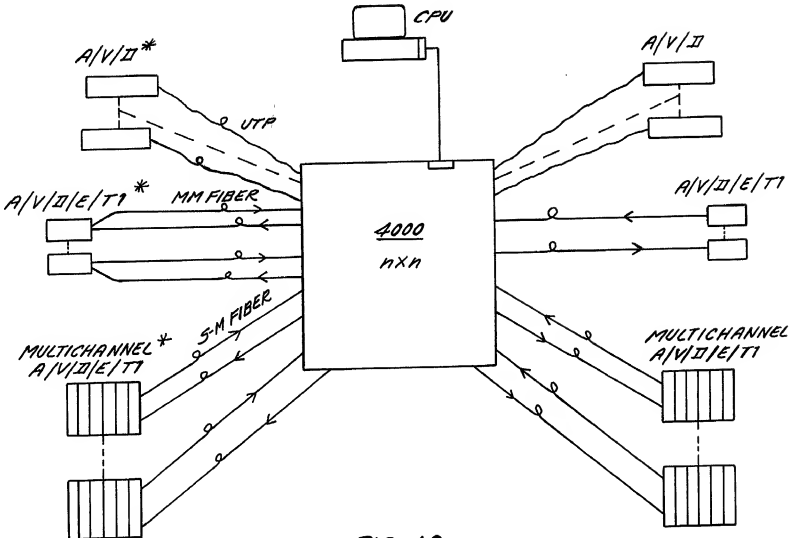


FIG. 40

09777970.020601

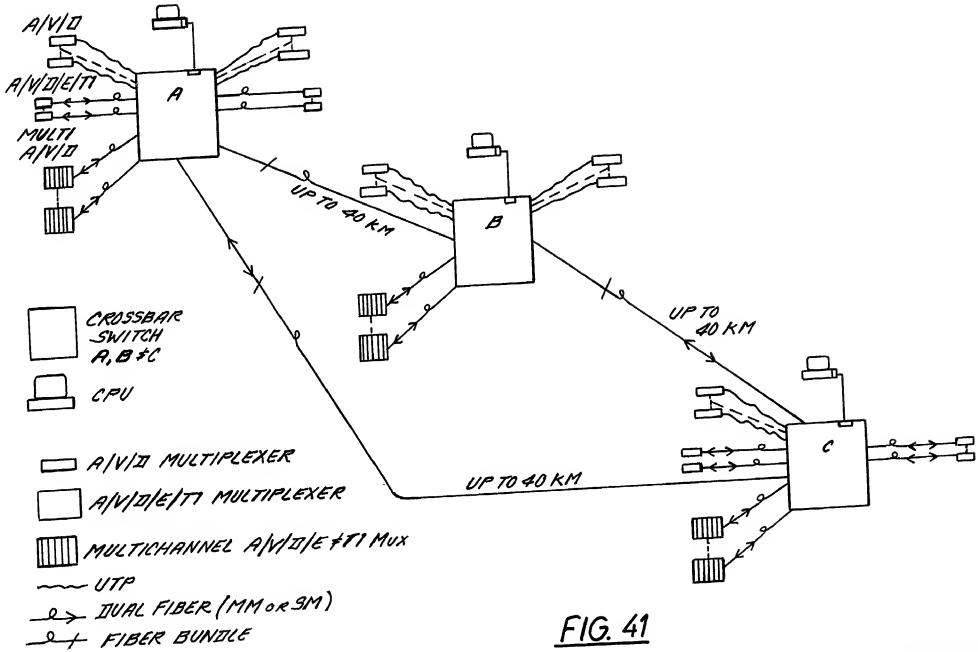


FIG. 41

TOSHIBA 0764260

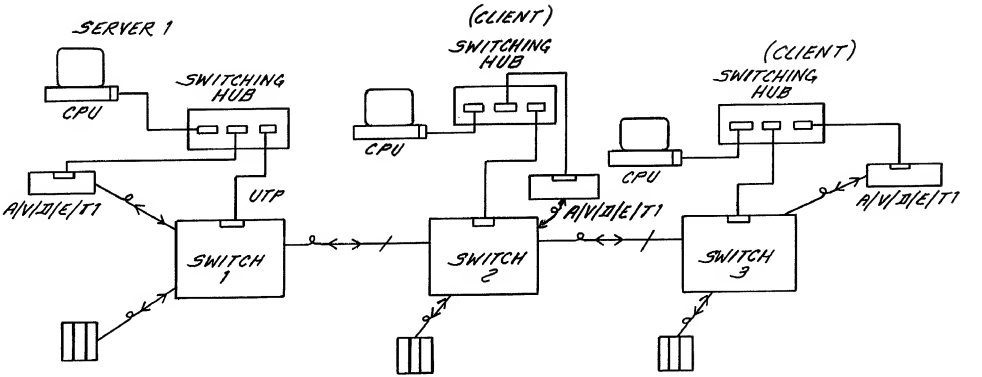


FIG. 42

09772760

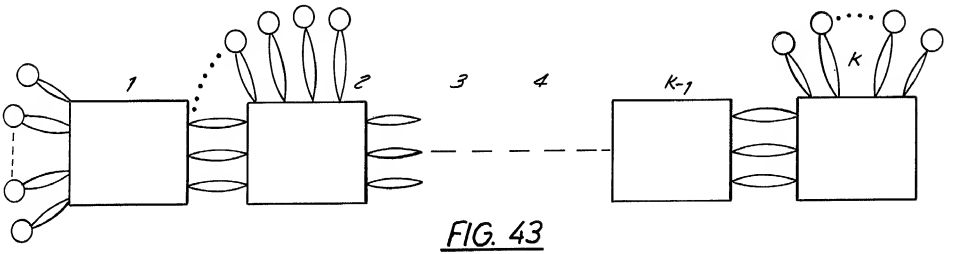


FIG. 43

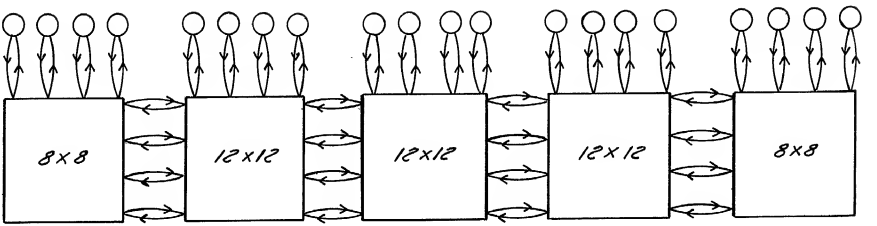


FIG. 44

09/779,760 07/09/2020

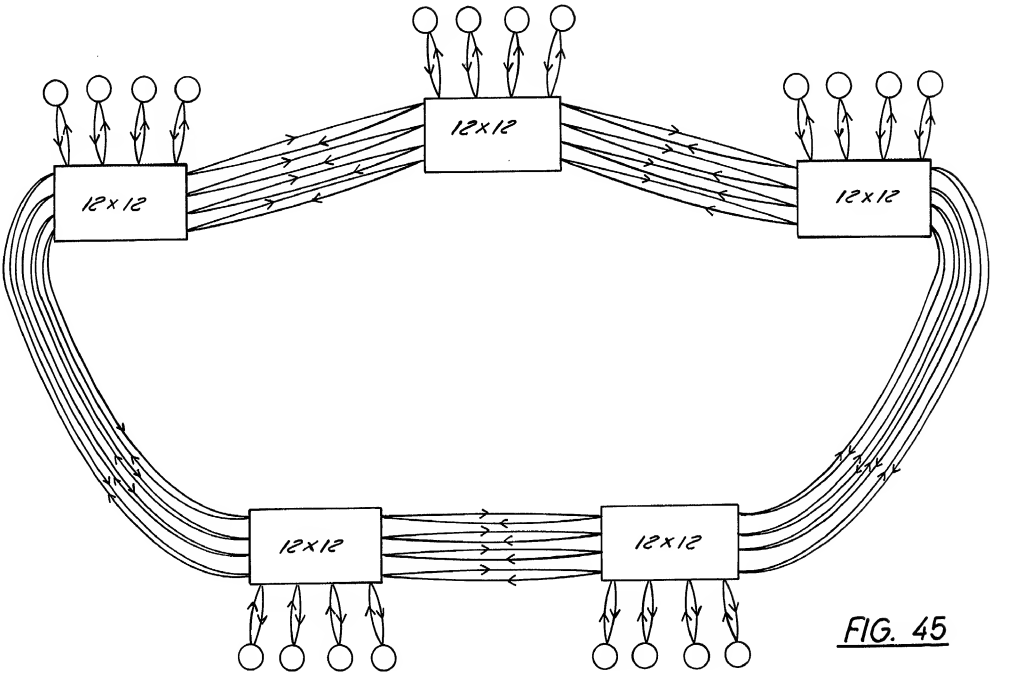


FIG. 45

09727970 "070601

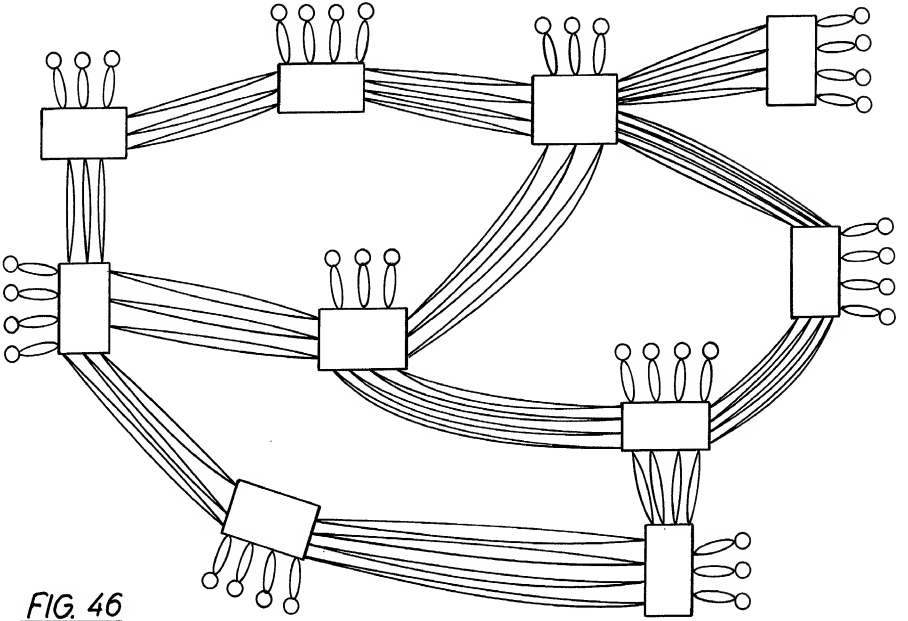


FIG. 46